DESIGN OF SECOND ORDER BUTTERWORTH HIGHPASS FILTER USING CMOS TECHNOLOGY

Anggraini Puspita Sari, Agung Darmawansyah, M. Julius St.

Abstract—The research Complementary Metal-Oxide Semiconductor (CMOS) Technology for Design of second order butterworth highpass filter IC. This is caused CMOS have excellence low power dissipation and small size. This research aims to know performance, quality and reliability second order butterworth highpass filter circuit. The method used to problem solving, analysis with the literature and the simulation use pspice program for exam the specification of circuit.

Index Terms—highpass filter, butterworth filter, CMOS Technology.

I. INTRODUCTION

In the recent years, semiconductor technology especially integrated circuit is the best choice to minimize the dimensions of a device. Considering the flexibility, low power requirements, and low cost, the incorporation of electronic components such as resistors, capacitors, transistors, diodes and other integrated circuit components allows for the creation of flexible and resilient chip designs. The technology applied to minimize the size of integrated circuit components is microelectronics technology. This technology is applied to realize the manufacture of small dimensional electronic circuits with consideration of increasing the capability of each component, weight reduction, strength of test power and the ability of stability to the environment. [1] [2] [3]

During this time, the evolution of CMOS technology more utilized in digital circuit but not so far for analog circuit. So in this research could explore for CMOS technology in analog circuit. [4]

In the field of analog electronics, filters are often used to reduce noise. One type of filter used is a highpass filter. The highpass filter passes all signal frequencies above the cut-off frequency and weakens all signals whose frequency is below the cut-off frequency. When designing a circuit requires a fast design technique and optimal layout to get the smallest possible size. In this research, we chose the layout of second order Butterworth filter IC using CMOS technology because it has advantages in low power dissipation and the size is very small. Power dissipation greatly affects workability, reliability, packaging, cost and brevity [1]. The type of Butterworth filter is selected to produce a maximal flat response on the passband portion.

II. RESEARCH METHODS

In this research will be designed a highpass filter with CMOS transistor. Fig. 1 shows the second order highpass filter circuit.

![Fig. 1 The Second Order Highpass Filter Circuit](image)

The operational amplifier (op-amp) used in this research is a second order op-amp CMOS with low power dissipation. Low power dissipation affects performance, reliability, packaging, cost, portability. This op-amp circuit consists of nine CMOS transistors and capacitors. The op-amp used in this research is a second order opamp CMOS with low power dissipation. Low power dissipation affects performance, reliability, packaging, cost, portability. This opamp circuit consists of nine CMOS transistors and a capacitor. The calculation of the values of each transistor is generated from the current analysis. The flowchart of design IC are shown Fig. 2.
III. CALCULATION RESULT OF HIGHPASS BUTTERWORTH FILTER IC

Before determining transistor comparison, the previously determined specifications CMOS operational amplifier second order is as follows: Gain Bandwidth (GB) = 2MHz, \( I_7 = 25\mu A \), \( V_{DD} = 5V \), \( V_{SS} = -5V \), \( \lambda_p = 0.02V^{-1} \), \( \lambda_n = 0.01V^{-1} \), \( V_{IN} = 0.8V \), \( V_{TP} = -0.8V \), \( K_N = 10\mu A/V^2 \), \( K_P = 4\mu A/V^2 \), \( C_L = 5pF \), \( V_{in\,(max)} = 3.5V \), \( V_{in\,(min)} = -2.5V \), \( R_{in} \approx \).

Fig. 2 The Flowchart Of Design IC

Fig. 3 shows a second order CMOS amplifier circuit.

The design procedure begins by calculating the value of the compensation capacitor (Cc). To obtain the comparison of \( g_{mi} \) and \( g_{m5} \) values based on the comparison of frequency amplification values of 3\( \omega_0 \) to obtain a ratio of 1/3.

\[
Cc = 3 \cdot C_L \frac{g_{mi}}{g_{m5}}
\]
\[
Cc = 3 \cdot 5 \cdot \frac{1}{3} = 5 \text{ pF}
\]

Then determined the minimum value of current \( I_7 = 25 \mu A \). Based on the specification of \( I_7 \) and the compensation capacitor calculation results obtained slew rate (SR).

\[
I_7 = SR \cdot Cc
\]
\[
25 \cdot 10^{-6} = SR \times 5 \cdot 10^{-12}
\]
\[
SR = 5 V/\mu s
\]

In design using microind with 0.8 \( \mu m \) CMOS Process. Based on the calculations that have been done then the size of all transistors are:

- \( L_1 = L_2 = 0.8 \mu m \)
  \( W_1 = W_2 = 15.8 \cdot 0.8 = 12.6 \mu m \)
- \( L_3 = L_4 = 0.8 \mu m \)
  \( W_3 = W_4 = 2.78 \cdot 0.8 = 2.2 \mu m \)
- \( L_5 = 0.8 \mu m \)
  \( W_5 = 31.3 \cdot 0.8 = 25 \mu m \)
- \( L_6 = 0.8 \mu m \)
  \( W_6 = 18 \cdot 0.8 = 14.4 \mu m \)
- \( L_7 = L_8 = 0.8 \mu m \)
  \( W_7 = W_8 = 3 \cdot 0.8 = 2.4 \mu m \)
- \( W_9 = 0.8 \mu m \)
  \( L_9 = 1.0 \cdot 0.8 = 0.8 \mu m \)
  \( L_9 = 8 \mu m \)

The value of power dissipation is:

\[
DP = (I_5 + I_7 + I_8) \cdot (V_{DD} - V_{SS})
\]
\[
= (150 \cdot 10^{-6} + 25 \cdot 10^{-6} + 25 \cdot 10^{-6}) \cdot (5 + 5)
\]
\[
= 2 \text{ mW}
\]

The calculation of low frequency gain is:

\[
A_d = 20 \log \frac{2 \cdot g_{m3} \cdot g_{m5}}{(\lambda_p + \lambda_n) I_7 (\lambda_p + \lambda_n) I_7}
\]
\[
= 20 \log \frac{2.6 \cdot 28 \cdot 10^{-5} \cdot 1.8 \cdot 10^{-4}}{0.03 \cdot 15 \cdot 10^{-3} \cdot 0.03 \cdot 25 \cdot 10^{-6}}
\]
\[
= 20 \log 6996.38
\]
\[
= 76.9 \text{ dB}
\]

The calculation of CMRR is:

\[
CMRR = 20 \log \frac{2 \cdot g_{m2} \cdot g_{m3}}{\lambda_p \cdot \lambda_n \cdot I_7 \cdot I_7}
\]
\[
= 20 \log \frac{2.62 \cdot 28 \cdot 10^{-6} \cdot 1.67 \cdot 10^{-5}}{0.02 \cdot 0.01 \cdot 12.5 \cdot 10^{-6} \cdot 25 \cdot 10^{-6}}
\]
\[
= 20 \log 33560
\]
\[
= 90.5 \text{ dB}
\]

In low frequencies, noise is caused by the bias currents and the asymmetry of components. In high frequencies, the noise is amplified again by the capacitance contained in the component, theoretically \( Ap = 1 \), then:

\[
PSRR = 20 \log \frac{A_d}{A_p}
\]
\[
= 20 \log 6996.38
\]
The value of the output voltage range can be calculated are:

- \( V_{\text{out(min)}} = V_{SS} + (V_{GS6} - V_{T6}) = -5 + 1.3 = -3.7\, V \)
- \( V_{\text{out(max)}} = V_{DD} - (V_{GS5} - V_{T}) = 5 - 1.5 = 3.5\, V \)

IV. SIMULATION RESULT

Second order highpass IC circuit simulation of differential mode gain configuration and common mode are shown in Fig. 4.

Based on the analysis of common mode gain, the ratio between the output voltage at point 5 to the input voltage at point 6 is 0.34403V shown in Fig. 5, so:

\[
A_c (\text{dB}) = 20 \log \frac{V_{\text{out}}}{V_{\text{in}}} = 20 \log 0.34403 = -9.2\, \text{dB}
\]

The value of CMRR is:

\[
\text{CMRR} = 20 \log \frac{A_d}{A_c} = A_d (\text{dB}) - A_c (\text{dB}) = 79 - (-9.2) = 88.2\, \text{dB}
\]

The circuitsimulation of PSRR positive (PSRR\(^+\)) and PSRR negative (PSRR\(^-\)) are shown in Fig.7.

\[
A_d (\text{dB}) = 20 \log \frac{V_{\text{out}}}{V_{\text{in}}} = 20 \log 8985.2
\]
Fig. 8 The Simulation Result of PSRR Graph

Fig. 8 shows the result of comparison of the output voltage at point 5 to the $V_{DP}$ voltage at point 10 is 513.504V, then:

$$A_{P}^{+} (\text{dB}) = 20 \log \frac{V_{out}}{V_{DP}}$$

$$= 20 \log 0.513504$$

$$= -5.8 \text{ dB}$$

So the value of PSRR is:

$$\text{PSRR}^{+} = Ad (\text{dB}) - A_{P}^{+} (\text{dB})$$

$$= 79 - (-5.8)$$

$$= 84.8 \text{ dB}$$

Fig. 9 The Simulation Result of PSRR Graph

Fig. 9 shows the result of comparison of the output voltage at point 5 to the $V_{DP}$ voltage at point 11 is 570.992mV, then:

$$A_{P}^{-} (\text{dB}) = 20 \log \frac{V_{out}}{V_{DP}}$$

$$= 20 \log 0.570992$$

$$= -4.8 \text{ dB}$$

So, the value of PSRR is:

$$\text{PSRR}^{-} = Ad (\text{dB}) - A_{P}^{-} (\text{dB})$$

$$= 79 - (-4.8)$$

$$= 83.8 \text{ dB}$$

The circuit simulation of slew rate positive (SR$^+$) and slew rate negative (SR$^-$) are shown in Fig. 10.

Fig. 10 The Circuit Simulation of SR$^+$ and SR$^-$

The Simulation Result of SR$^+$ Graph are shown Fig. 11 and the value of SR$^-$ is:

$$\text{SR}^- = \frac{V_{max} - V_{min}}{\Delta t}$$

$$= \frac{4.7493 - (-5)}{3.913 \times 10^{-6} - 1.10^{-6}}$$

$$= 3.35 \text{ V/μs}$$

Fig. 11 The Simulation Result of SR$^-$ Graph

Fig. 12 The Simulation Result of SR Graph
Fig. 12 shows a The Simulation Result of SR Graph and the value of SR is:

\[ SR = \frac{V_{max} - V_{min}}{\Delta t} \]

\[ = \frac{-4.9676 - 4.7967}{3.9826 \times 10^{-6} - 1.10^{-6}} \]

\[ = -3.27 \text{ V/\(\mu\)s} \]

The second order highpass filter circuit are shown in Fig. 13.

---

**Fig. 13 The Second Order Highpass Filter Circuit**

---

**Fig. 14 Graph of Frequency Response of Second Order Highpass Filter**

Fig. 14 shows a Graph of Frequency Response of Second Order Highpass Filter when \( f_0 = 1 \text{kHz} \). At \( f_0 = 1 \text{kHz} \), the voltage gain \((A_0)\) is equal to 0.709 V.

Fig. 15 shows the graph of response frequency highpass filter (in dB) at \( f_0 = 1 \text{kHz} \). Pada saat \( f_0 = 1 \text{kHz} \) penguatan tegangan \( A_0 \) sama dengan -2.99dB.

---

**Fig. 15 The Graph of Response Frequency Highpass Filter (in dB) at \( f_0 = 1 \text{kHz} \)**

---

**Fig. 16 The Graph of Second Order Highpass Filter Phase At \( f_0 = 1 \text{kHz} \)**

Fig. 16 shows the magnitude of the gain (in dB), which occurs at \( f_0 \) is -2.99 dB with a phase angle of 88.25°.

Fig. 17 shows the results of highpass filter IC use Microwind. The IC area is 1110μm x 385μm.

---

**Fig. 17 The Results of Highpass Filter IC Use Microwind**

---

**Table 1. Calculation and Simulation Result to Second Order Op-amp CMOS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Calculation Results</th>
<th>Simulation Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>( A_d )</td>
<td>76.9 dB</td>
<td>79 dB</td>
</tr>
<tr>
<td>SR</td>
<td>5 V/(\mu)s</td>
<td>3.35V/(\mu)s</td>
</tr>
<tr>
<td>CMRR</td>
<td>90.5 dB</td>
<td>88.2dB</td>
</tr>
<tr>
<td>PSRR</td>
<td>76.9 dB</td>
<td>84.8dB</td>
</tr>
<tr>
<td>PD</td>
<td>2 mW</td>
<td>2.28mW</td>
</tr>
<tr>
<td>( V_o )</td>
<td>-3.7 V/s/d 3.5 V</td>
<td>-5 V/s/d 4.7542V</td>
</tr>
</tbody>
</table>

**Table 2. Result of Design IC and IC GH580**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Design Results</th>
<th>IC GH580</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Highpass</td>
<td>Highpass</td>
</tr>
<tr>
<td>Order</td>
<td>Dua</td>
<td>Dua</td>
</tr>
<tr>
<td>Type</td>
<td>Butterworth</td>
<td>Butterworth</td>
</tr>
<tr>
<td>PD</td>
<td>2.28mW</td>
<td>25mW</td>
</tr>
<tr>
<td>PSRR</td>
<td>83.8dB</td>
<td>56dB</td>
</tr>
</tbody>
</table>
V. CONCLUSION

The conclusion of this research are input signal given in highpass filter circuit above cutoff frequency will be passed while below cutoff frequency will be damped, design result for CMOS amplifier and second order highpass filter can be fabricated due to shift of cutoff frequency and voltage gain close to expected that is for frequency cutoff = 1kHz and voltage gain (Ao) = 0.707V or -3dB, the design excellence IC is having a small power dissipation value of 2.28mW compared to the second order IC GH580, the results of design second order highpass IC use Microwind have IC area is 1110μm x 385μm.

REFERENCES