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DESIGN OF SECOND ORDER BUTTERWORTH HIGHPASS FILTER USING CMOS TECHNOLOGY

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***Abstract*—The research Complementary Metal-Oxide Semiconductor (CMOS) Technology for Design of second order butterworth highpass filter IC. This is caused CMOS have excellence low power dissipation and small size. This research aims to know performance, quality and reliability second order butterworth highpass filter circuit. The method used to problem solving, analysis with the literature and the simulation use pspice program for exam the specification of circuit. To make IC picture using DSCH software and layout circuit using Microwind program. From examination result -2,99dB for gain voltage parameter, frequency -40dB and 88,25° phase shift second order highpass filter. The result of this circuit have low power dissipation although applied to second order highpass filter equal 2,28mW better than generality IC second order highpass filter (GH580). Wide of layout circuit is 1110µm x 385µm.**

Index Terms— highpass filter, butterworth filter, CMOS Technology.

I. INTRODUCTION

IN the recent years, semiconductor technology especially integrated circuit is the best choice to minimize the dimensions of a device. Considering the flexibility, low power requirements, and low cost, the incorporation of electronic components such as resistors, capacitors, transistors, diodes and other integrated circuit components allows for the creation of flexible and resilient chip designs. The technology applied to minimize the size of integrated circuit components is microelectronics technology. This technology is applied to realize the manufacture of small dimensional electronic circuits with consideration of increasing the capability of each component, weight reduction, strength of test power and the ability of stability to the environment.[1] [2][3]

During this time, the evolution of CMOS technology more utilized in digital circuit but not so far for analog circuit. So in this research could explore for CMOS technology in analog circuit.[4]

In the field of analog electronics, filters are often used to reduce noise. One type of filter used is a highpass filter. The highpass filter passes all signal frequencies above the cut-off frequency and weakens all signals whose frequency is below the cut-off frequency. When designing a circuit requires a fast design technique and optimal layout to get the smallest possible size. In this research, we chose the layout of second order Butterworth filter IC using CMOS technology because it has advantages in low power dissipation and the size is very small. Power dissipation greatly affects workability, reliability, packaging, cost and brevity [1]. The type of Butterworth filter is selected to produce a maximal flat response on the passband portion.

II. REASERCH METODS

In this research will be designed a highpass filter with CMOS transistor. Fig. 1 shows the second order highpass filter circuit.

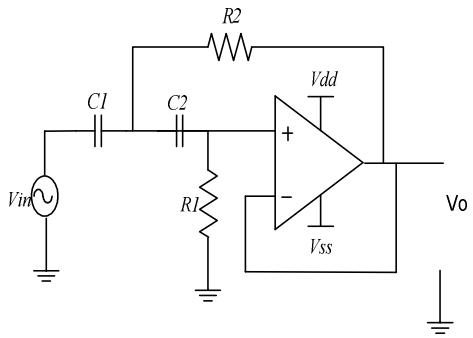

Fig. 1 The Second Order Highpass Filter Circuit

The operational amplifier (op-amp) used in this research is a second order op-amp CMOS with low power dissipation. Low power dissipation affects performance, reliability, packaging, cost, portability. This op-amp circuit consists of nine CMOS transistors and capacitors. The op-amp used in this research is a second order opamp CMOS with low power dissipation. Low power dissipation affects performance, reliability, packaging, cost, portability. This opamp circuit consists of nine CMOS transistors and a capacitor. The calculation of the values of each transistor is generated from the current analysis. The flowchart of design IC are shown Fig. 2

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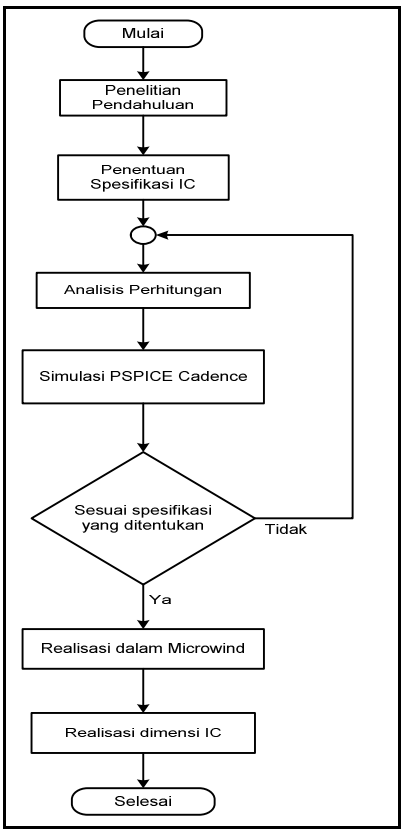

Fig. 2 The Flowchart Of Design IC

III. CALCULATION RESULT OF HIGHPASS BUTTERWORTH FILTER IC

Before determining transistor comparison, the previously determined specifications CMOS operational amplifier second order is as follows: Gain Bandwidth (GB) = 2MHz, I_7= 25µA, V_{DD}=5V, V_{SS}= -5V, λ_P = 0,02V^{-1}, λ_N= 0,01V^{-1}, V_{TN}= 0,8V, V_{TP}= -0,8V, K_N=10µA/V^2, K_P= 4µA/V^2, C_L= 5pF, $V_{in\ (maks)}$= 3,5 V,$V_{in\ (min)}$= -2,5V, R_{in}= ~.[2]

Fig. 3 shows a second order CMOS amplifier circuitada

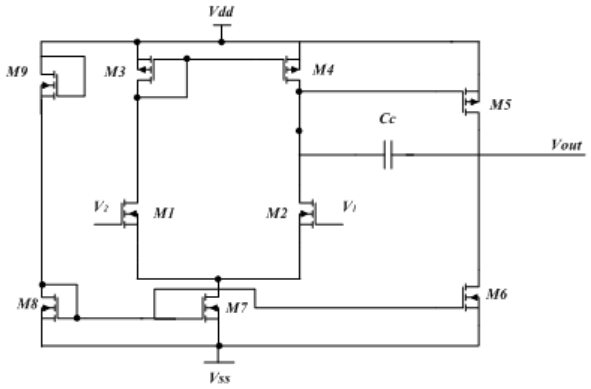

Fig. 3 Second Order CMOS Amplifier Circuit

The design procedure begins by calculating the value of the compensation capacitor (Cc). To obtain the comparison of gmi and gm5 values based on the comparison of frequency amplification values of 3ω0 to obtain a ratio of 1/3.

$$Cc = 3 \,.\, C_L \frac{g_{mi}}{g_{m5}}$$

$$Cc = 3 \,.\, 5 \,.\, \frac{1}{3} = 5 \text{ pF}$$

Then determined the minimum value of current I7 = 25 µA. Based on the specification of I7 and the compensation capacitor calculation results obtained slew rate (SR).

$$I_7 = SR \,.\, Cc$$

$$25.10^{-6} = SR \times 5.10^{-12}$$

$$SR = 5 \text{ V}/\mu\text{s}$$

In design using microwind with 0.8 µm CMOS Process. [2][3]Based on the calculations that have been done then the size of all transistors are:

- L1 = L2 = 0,8 µm
  W1 = W2 = 15,8.0,8 = 12,6µm
- L3 =L4 = 0,8 µm
  W3 = W4 = 2,78.0,8 = 2,2µm
- L5 = 0,8 µm
  W5 = 31,3..0,8 = 25µm
- L6 = 0,8 µm
  W6 = 18.0,8 = 14,4µm
- L7 = L8 = 0,8 µm
  W7 = W8 = 3.0,8 = 2,4µm
- W9 = 0,8 µm

$$L9 = \frac{0.8.10^{-6}}{0.1} = 8\mu m$$

The value of power dissipation is:

$$DP = (I_5 + I_7 + I_8) \,.\, (V_{DD} - V_{SS})$$
$$= (150.10^{-6} + 25.10^{-6} + 25.10^{-6}) \,.\, (5 + 5)$$
$$= 2 \text{ mW}$$

The calculation of low frequency gain is :

$$A_d = 20 \log \frac{2.g_{m2} g_{m5}}{(\lambda_P + \lambda_N) I_5 (\lambda_P + \lambda_N) I_7}$$

$$= 20 \log \frac{2.6,28.10^{-5}.1,88.10^{-4}}{0,03.0,15.10^{-3}.0,03.25.10^{-6}}$$
$$= 20 \log 6996,38$$
$$= 76,9 \text{ dB}$$

The calculation of CMRR is:

$$CMRR = 20 \log \frac{2.g_{m2} g_{m3}}{\lambda_P \lambda_N I_3 I_7}$$

$$= 20 \log \frac{2.62,8.10^{-6}.1,67.10^{-5}}{0,02.0,01.12,5.10^{-6}.25.10^{-6}}$$
$$= 20 \log 33560$$
$$= 90,5 \text{ dB}$$

In low frequencies, noise is caused by the bias currents and the asymmetry of components. In high frequencies, the noise is amplified again by the capacitance contained in the component, theoretically Ap = 1, then:

$$PSRR = 20 \log \frac{A_d}{A_P}$$
$$= 20 \log 6996,38$$

= 76,9 dB

The value of the output voltage range can be calculated are :

$V_{out(min)} = V_{SS} + (V_{GS6}-V_{T6})$
$= -5 + 1,3$
$= -3,7V$
$V_{out(max)} = V_{DD}-(V_{SG5}-V_T)$
$= 5-1,5$
$= 3,5$ V.

IV. SIMULATION RESULT

Second order highpass IC circuit simulation of differential mode gain configuration and common mode are shown in Fig. 4.

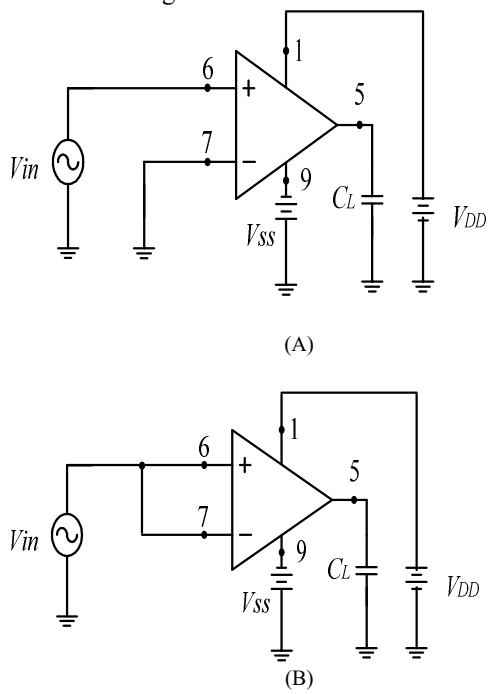

Fig 4. Differential Mode Gain Configuration (A) And Common Mode (B)

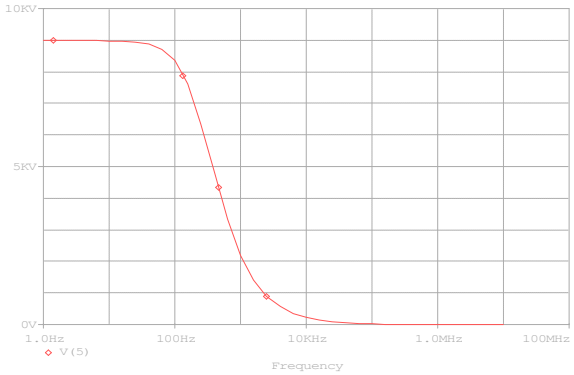

Fig. 5 shows adifferential mode gain graph.

The total power dissipation of the second order CMOS amplifier is 2.28 mW. Strengthening the voltage, the ratio between the output voltage at point 5 to the input voltage at point 6 is 8985.2V shown in Fig. 5, so:

$$\text{Ad (dB)} = 20 \log \frac{Vout}{Vin}$$
$$= 20 \log 8985,2$$

= 79 dB

Fig. 6 shows a common mode gain graph

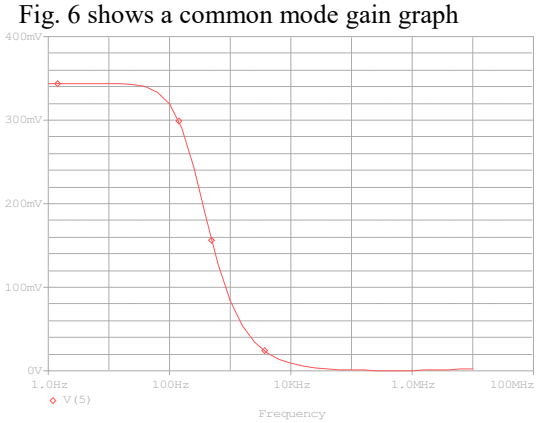

Fig. 6 Common Mode Gain Graph

Based on the analysis of common mode gain, the ratio between the output voltage at point 5 to the input voltage at point 6 is 0.34403V so:

$$\text{Ac (dB)} = 20 \log \frac{Vout}{Vin}$$
$$= 20 \log 0,34403$$
$$= -9,2 \text{ dB}$$

The value of CMRR is:

$$\text{CMRR} = 20 \log \frac{Ad}{Ac}$$
$$= \text{Ad (dB)} - \text{Ac (dB)}$$
$$= 79 - (-9,2)$$
$$= 88,2\text{dB}$$

The circuitsimulation of PSRR positive ($PSRR^+$) and PSRR negative ($PSRR^-$) are shown in Fig.7.

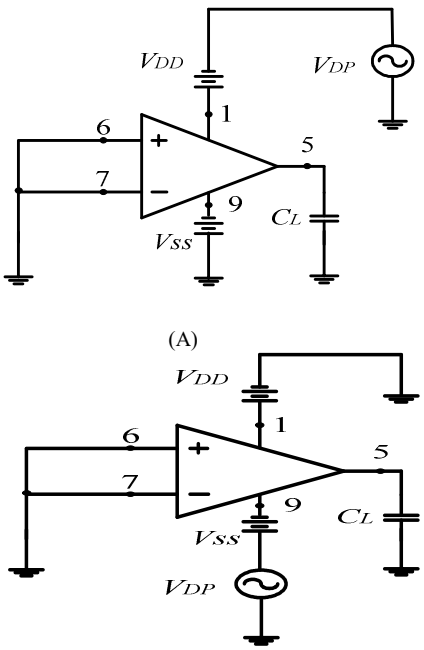

Fig.7 The Circuit Simulation of $PSRR^+$ and $PSRR^-$

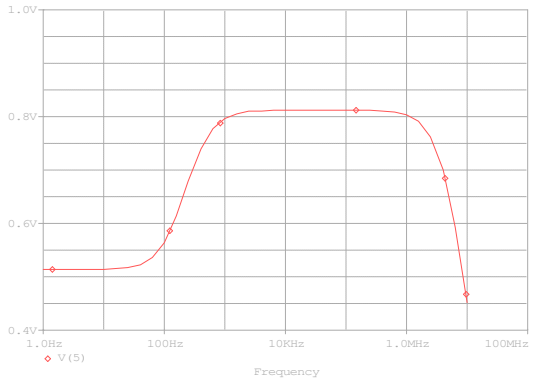

Fig. 8 The Simulation Result of PSRR$^+$Graph

Fig. 8 shows a the result of comparison of the output voltage at point 5 to the V_{DP} voltage at point 10 is 513.504V, then:

$$Ap^+ (dB) = 20 \log \frac{Vout}{V_{DP}}$$
$$= 20 \log 0{,}513504$$
$$= -5{,}8 \text{ dB}$$

So the value of PSRR$^+$is:

$$PSRR^+ = Ad (dB) - A_P{}^+ (dB)$$
$$= 79 - (-5{,}8)$$
$$= 84{,}8 \text{ dB}$$

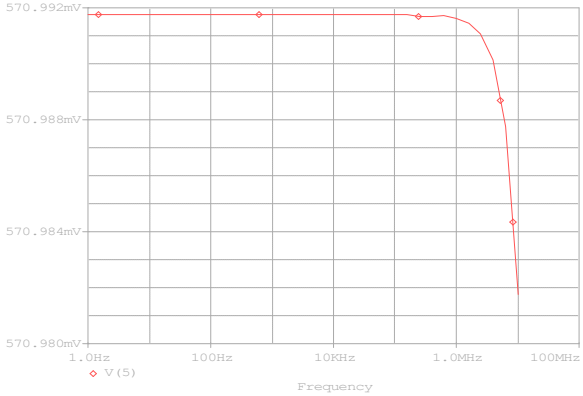

Fig. 9 The Simulation Result of PSRR$^-$Graph

Fig.9 shows a the result of comparison of the output voltage at point 5 to the V_{DP} voltage at point 11 is 570.992mV, then:

$$Ap^- (dB) = 20 \log \frac{Vout}{V_{DP}}$$
$$= 20 \log 0{,}570992$$
$$= -4{,}8 \text{ dB}$$

So, the value of PSRR$^-$is:

$$PSRR^- = Ad (dB) - A_P{}^- (dB)$$
$$= 79 - (-4{,}8)$$
$$= 83{,}8 \text{ dB}$$

The circuit simulation of slew rate positive (SR^+) and slew rate negative (SR^-) are shown in Fig. 10.

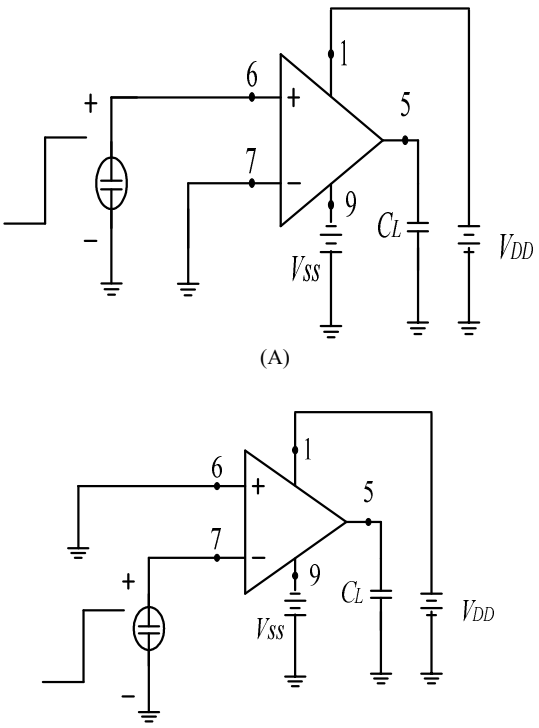

Fig. 10 The Circuit Simulation of SR$^+$ and SR$^-$

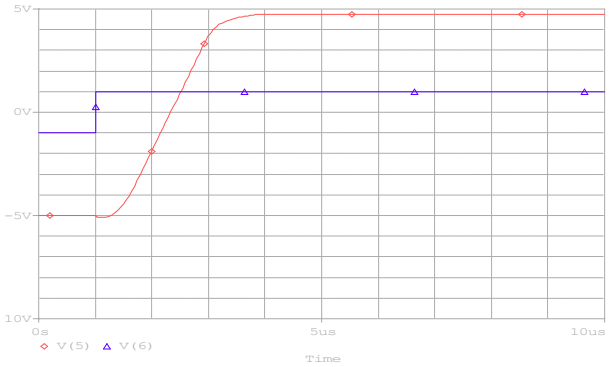

Fig.11 The Simulation Result of SR$^+$Graph

The Simulation Result of SR^+ Graph are shown Fig.11 andthe value of SR$^+$is:

$$SR^+ = \frac{Vmaks - V\min}{\Delta t}$$
$$= \frac{4{,}7493 - (-5)}{3{,}913.10^{-6} - 1.10^{-6}}$$
$$= 3{,}35 \text{ V/µs}$$

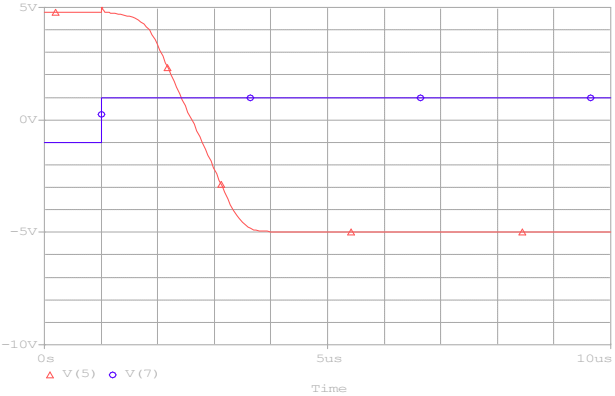

Fig. 12 The Simulation Result of SR$^-$Graph

Fig. 12 shows a The Simulation Result of SR- Graph and the value of SR- is:

$$SR^- = \frac{Vmaks - V\min}{\Delta t}$$
$$= \frac{-4{,}9676 \; - 4{,}7967}{3{,}9826 \; .10^{-6} - 1.10^{-6}}$$
$$= -3{,}27 \text{ V/µs}$$

The second order highpass filter circuit are shown in Fig. 13.

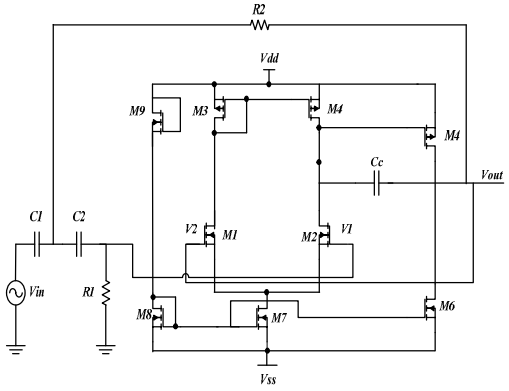

Fig.13 The Second Order Highpass Filter Circuit

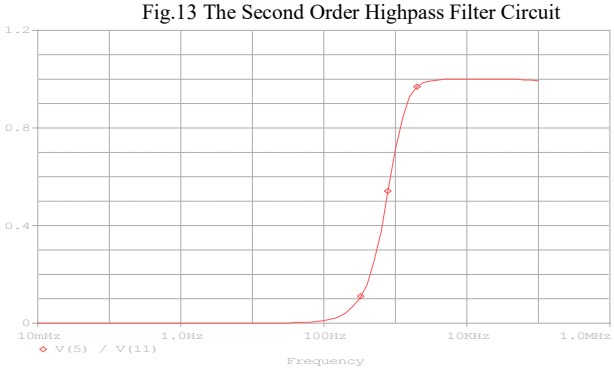

Fig. 14 Graph of Frequency Response of Second Order Highpass Filter at fo = 1kHz

Fig. 14 shows a Graph of Frequency Response of Second Order Highpass Filter when fo = 1kHz.Atfo = 1kHz, the voltage gain (A_0) is equal to 0.709 V.

Fig. 15shows athe graph of response frequency highpass filter (in dB) at fo = 1 kHz. Pada saat fo = 1 kHz penguatan tegangan Ao sama dengan -2,99dB.

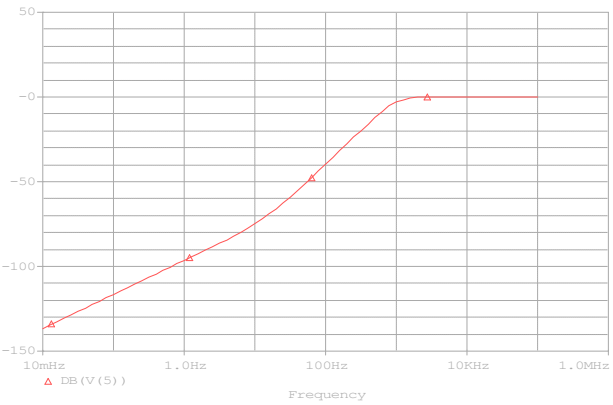

Fig. 15 The Graph of Response Frequency Highpass Filter (in dB) at fo = 1 kHz

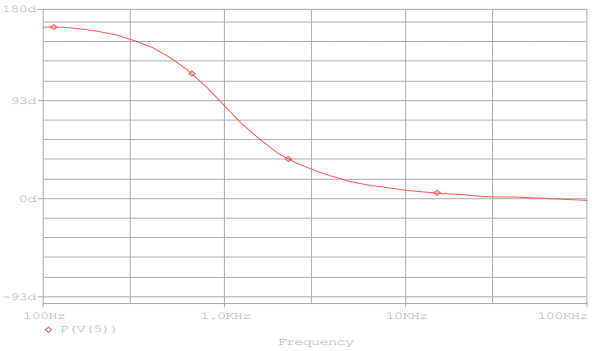

Fig. 16 The Graph of Second Order Highpass Filter Phase At fo = 1kHz

Fig.16shows the magnitude of the gain (in dB), which occurs at fo is -2.99 dB with a phase angle of 88.25°.

Fig.17shows the results of highpass filter IC use Microwind. The IC area is 1110µm x 385µm.

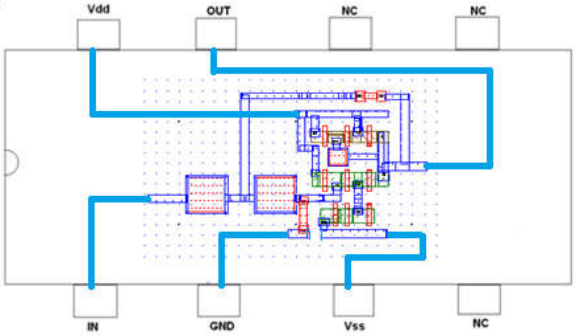

Fig. 17 The Results of Highpass Filter IC Use Microwind

Table 1 shows a Calculation and Simulation Result to Second Order Op-amp CMOS and Table 2 shows a Result of Design IC and IC GH580.

Table1.Calculation and Simulation Result to Second Order Op-amp CMOS

Parameter	Calculation Results	Simulation Results
Ad	76,9 dB	79dB
SR	5 V/µs	3,35V/µs
CMRR	90,5 dB	88,2dB
PSRR	76,9 dB	84,8dB
PD	2 mW	2,28mW
V_o	-3,7 V s/d 3,5 V	-5V s/d 4,7542V

Table 2.Result of Design IC and IC GH580

Parameter	Design Results	IC GH580
Type	Highpass	Highpass
Order	Dua	Dua
Type	Butterworth	Butterworth
PD	2,28mW	25mW
PSRR	83,8dB	56dB

V. CONCLUTION

The conclusion of this research are input signal given in highpass filter circuit above cutoff frequency will be passed while below cutoff frequency will be damped, design result for CMOS amplifier and second order highpass filter can be fabricated due to shift of cutoff frequency and voltage gain close to expected that is for frequency cutoff = 1kHz and voltage gain (Ao) = 0.707V or -3dB, the design excellence IC is having a small power dissipation value of 2.28mW compared to the second order IC GH580, the results of design second order highpass IC use Microwind have IC area is 1110µm x 385µm.

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